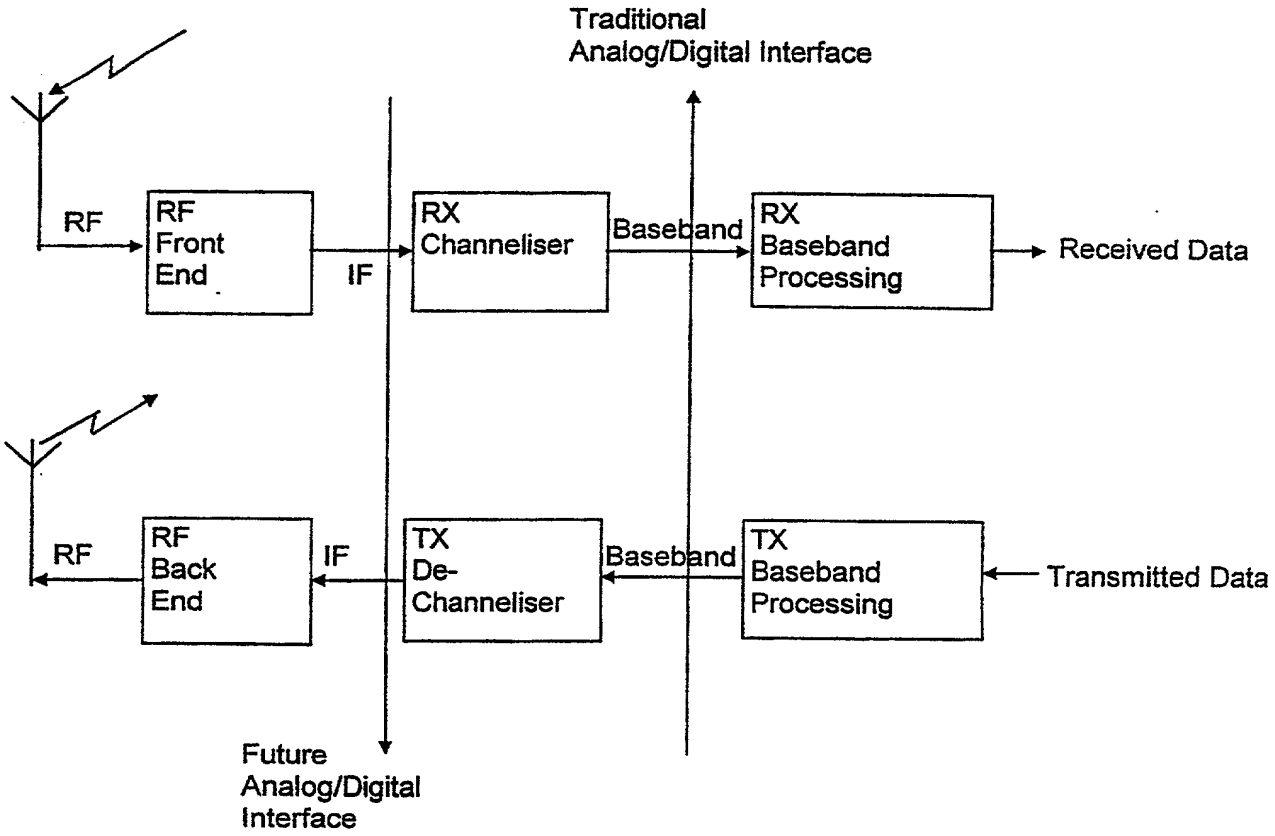

Fig. 1

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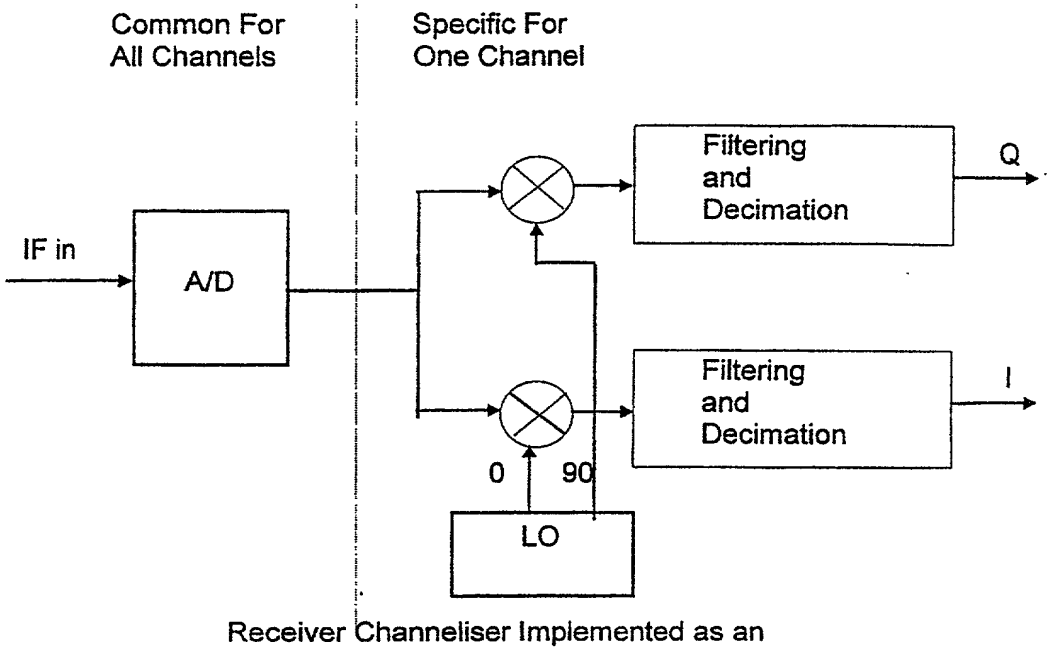

Receiver Channeliser Implemented as an IQ Channeliser

Fig 2

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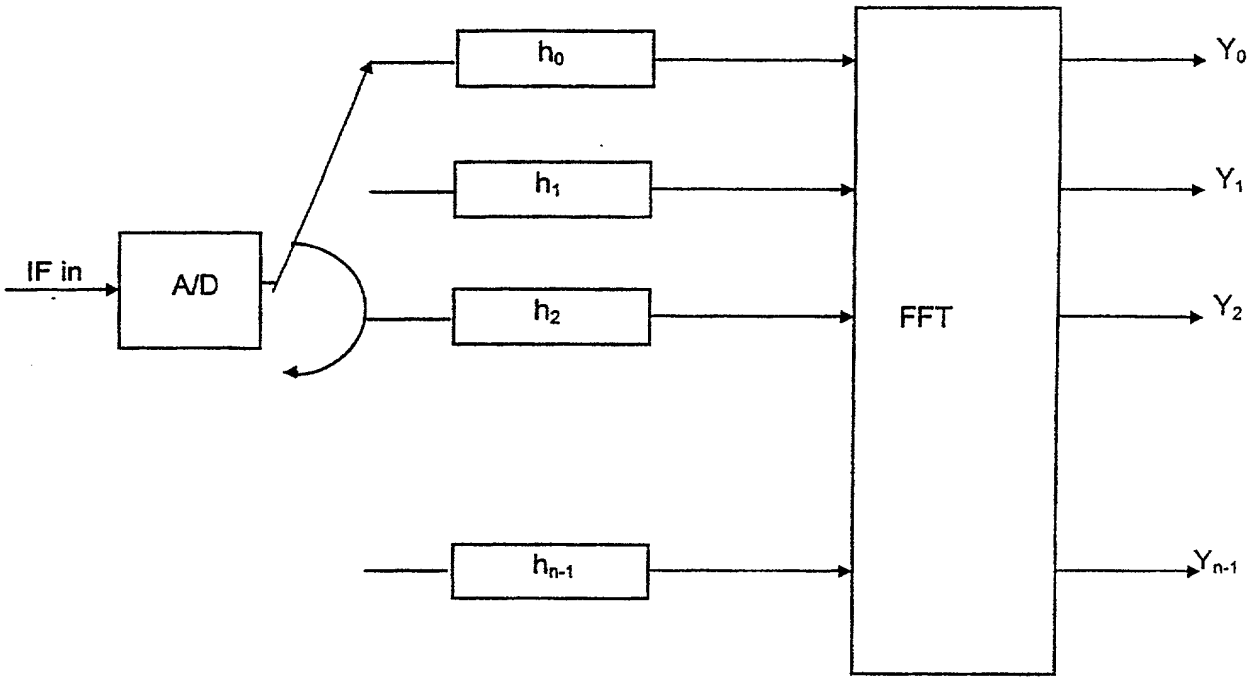

Receiver Channeliser Implemented Via
A Decimated Filter Bank

Fig. 3

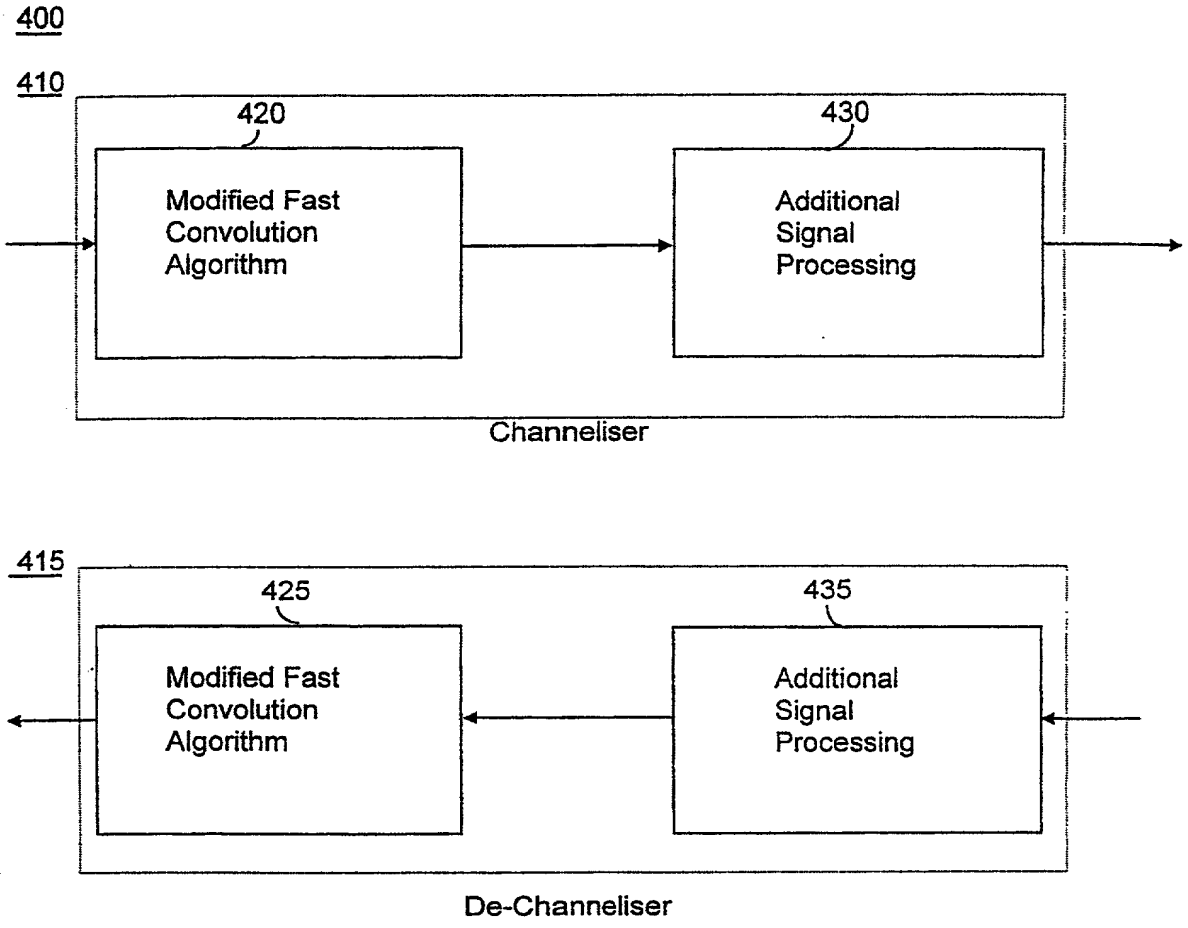

Fig. 4

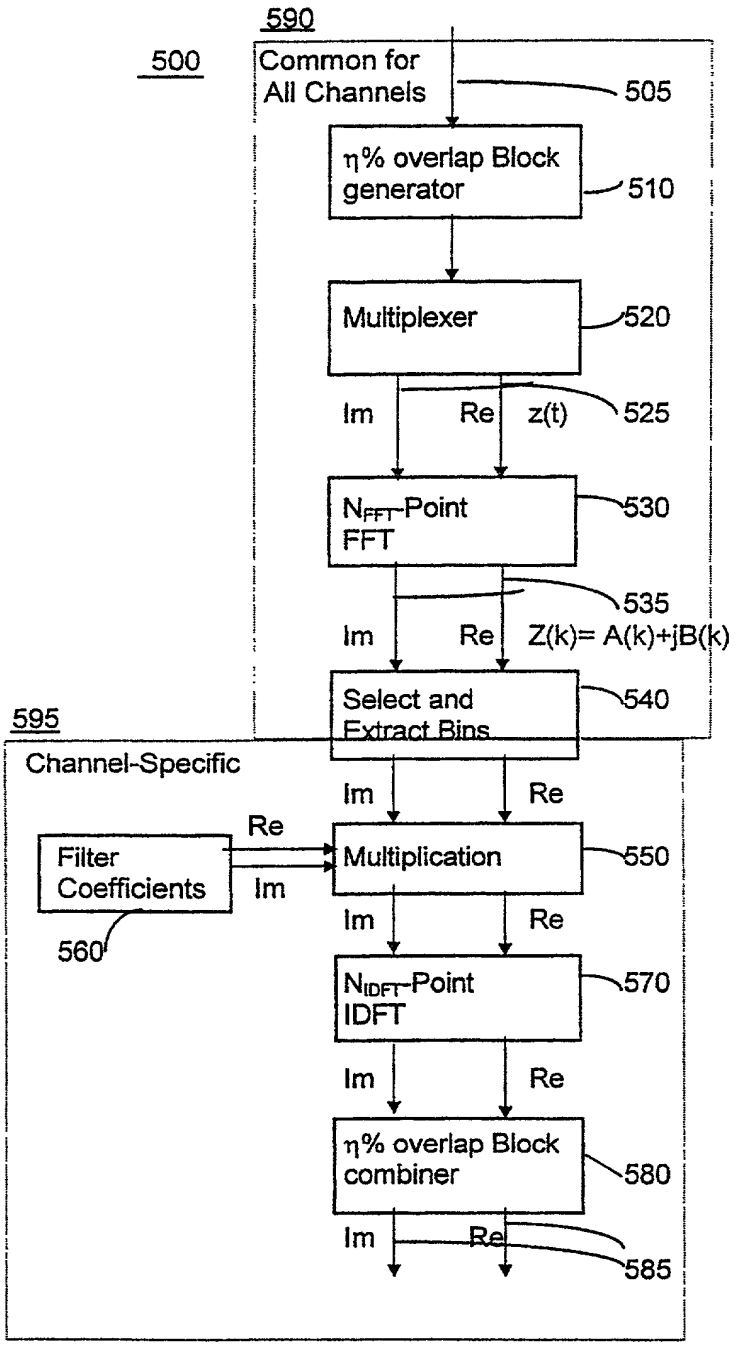
590
500
Common for All Channels
505
η% overlap Block generator
510
Multiplexer
520
Im
Re
z(t)
525
N_{FFT}-Point FFT
530
535
Im
Re
Z(k)= A(k)+jB(k)
Select and Extract Bins
540
595
Channel-Specific
Im
Re
Re
Filter Coefficients
Im
Multiplication
550
560
Im
Re
N_{IDFT}-Point IDFT
570
Im
Re
η% overlap Block combiner
580
Im
Re
585

Fig. 5

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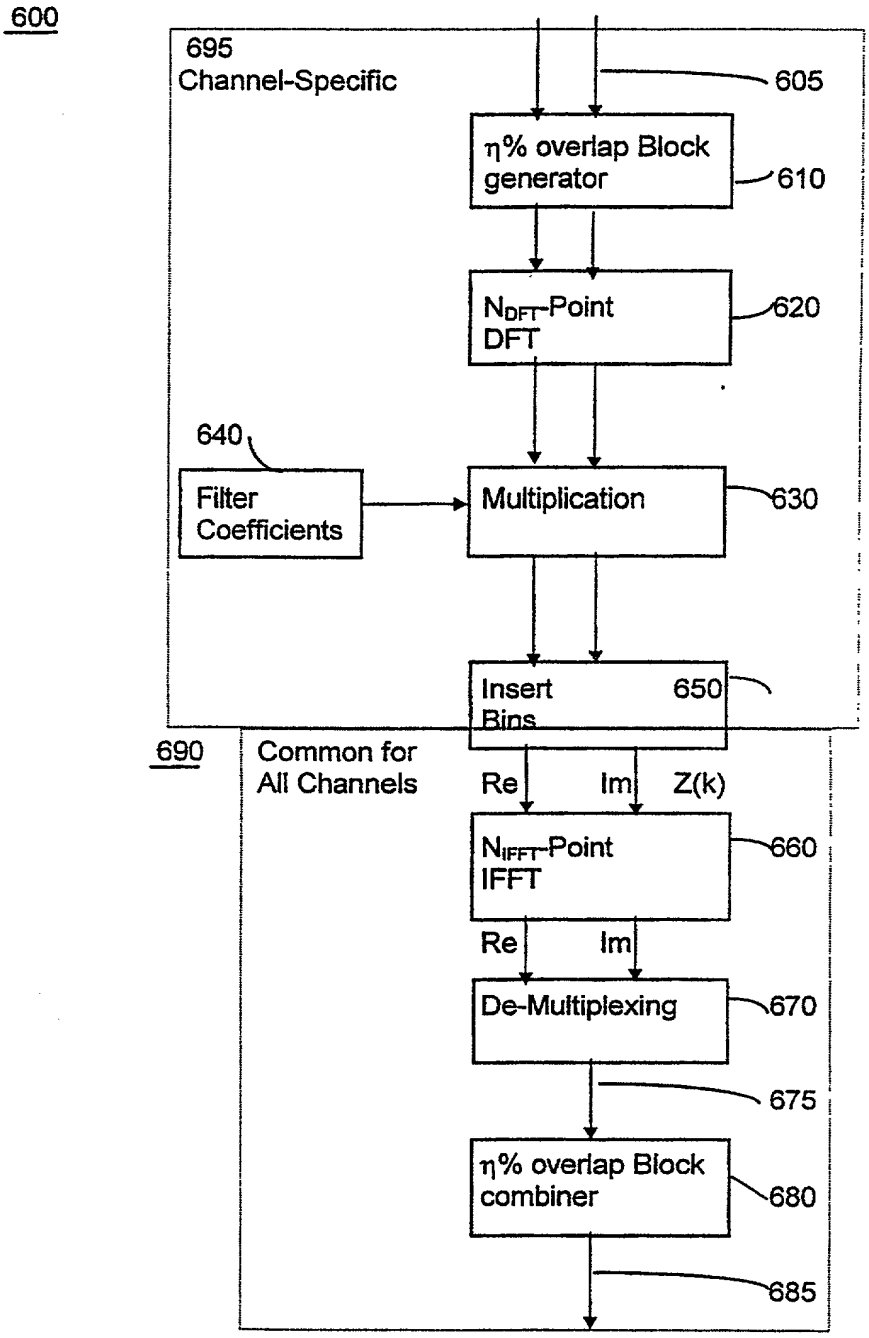
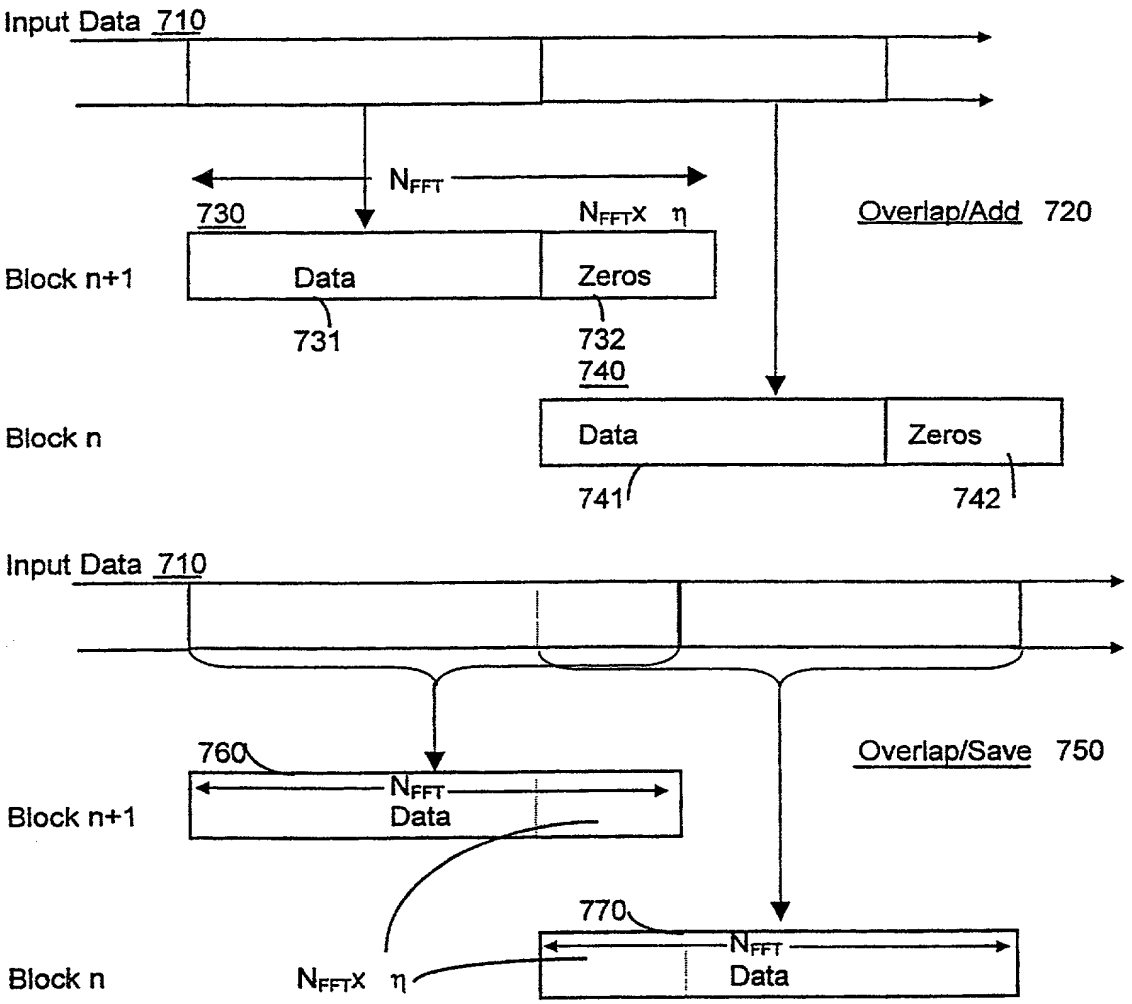


Fig. 6



η% Overlap Block Generator

Fig. 7

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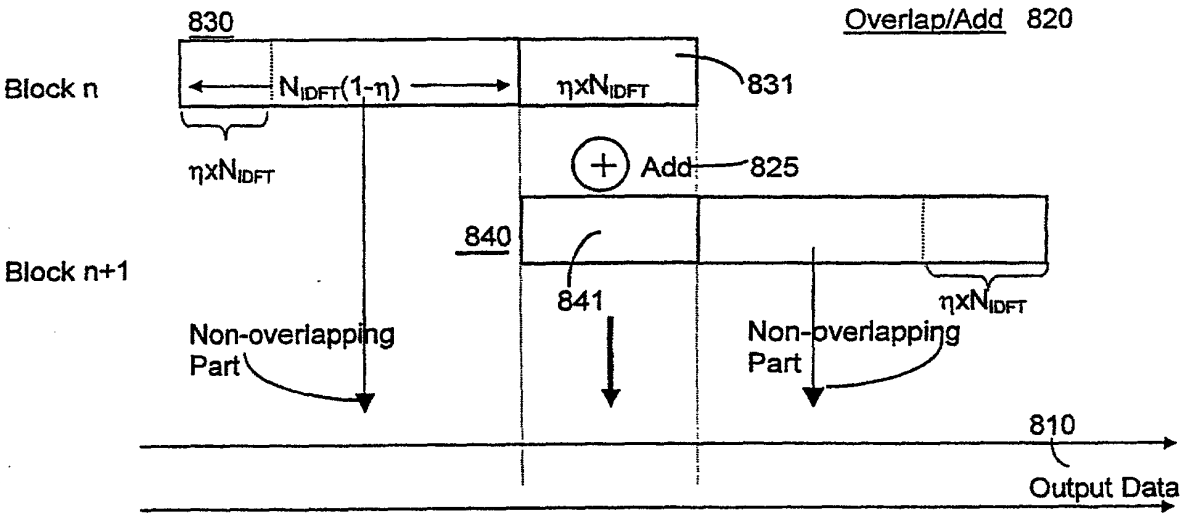

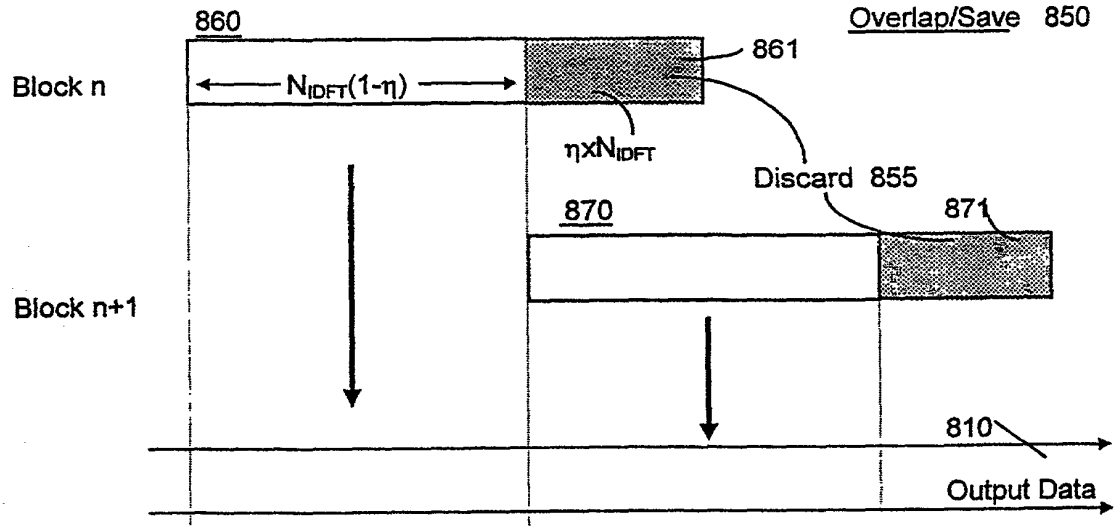

η% Overlap Block Combiner

Fig. 8

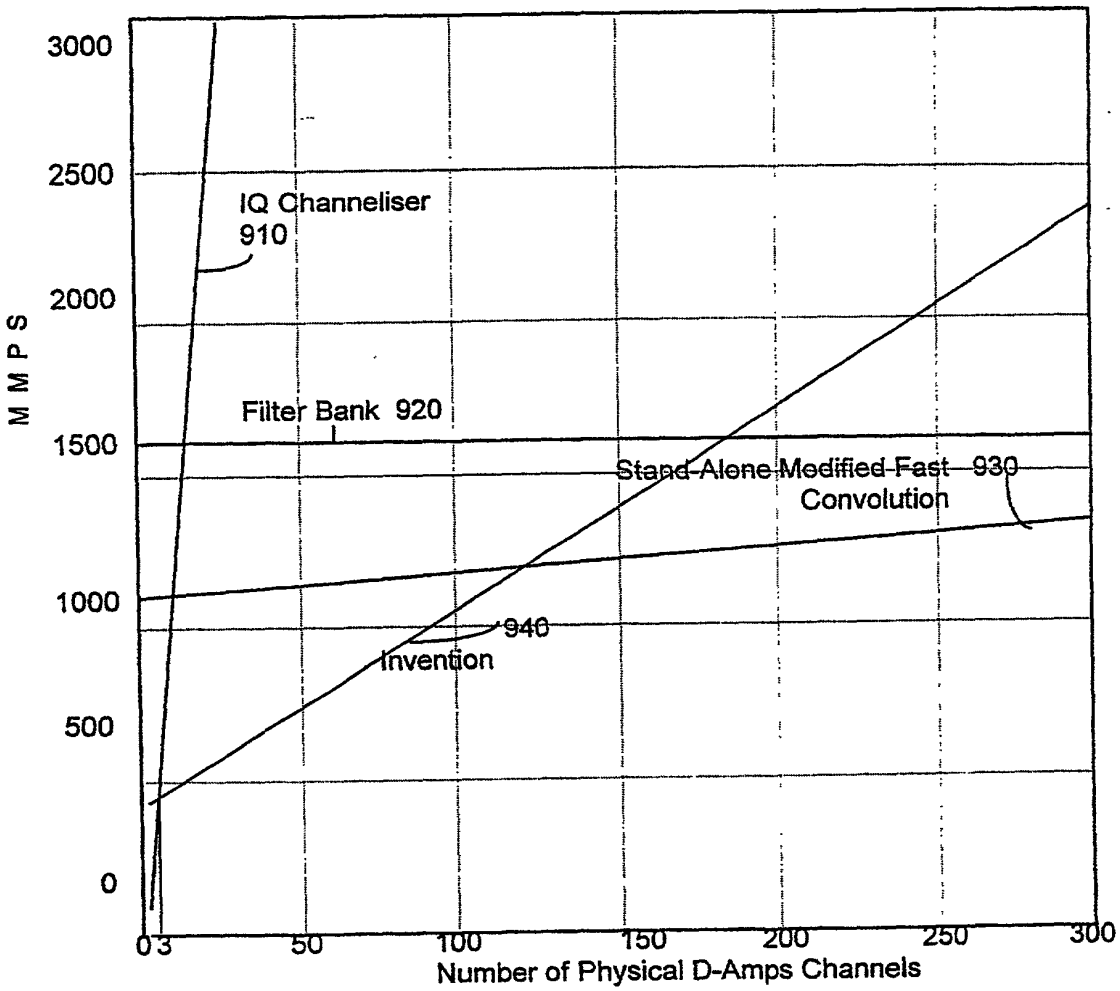

Fig. 9

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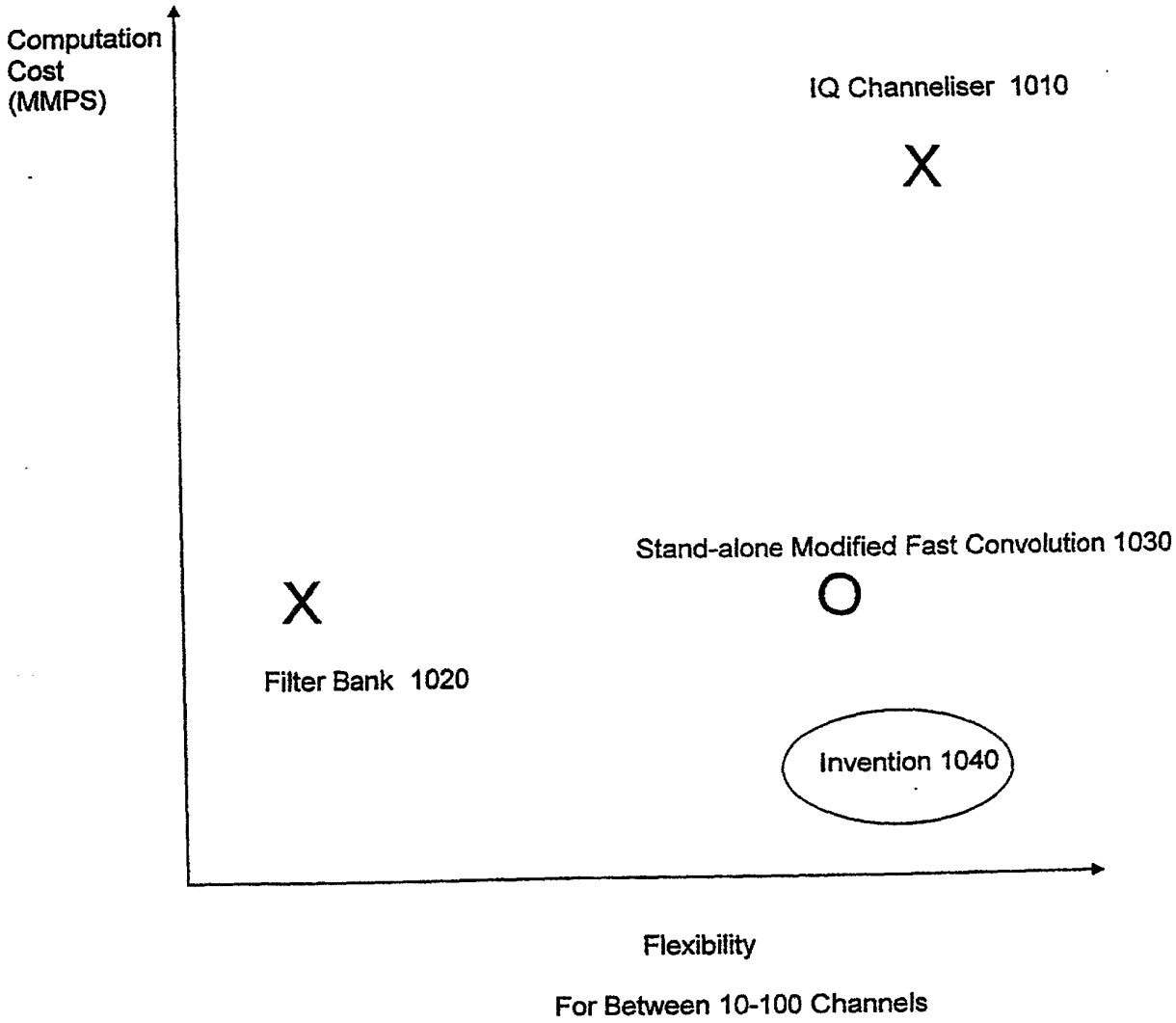
Computation Cost (MMPS)
IQ Channeliser 1010
X
Stand-alone Modified Fast Convolution 1030
O
X
Filter Bank 1020
Invention 1040
Flexibility
For Between 10-100 Channels

Fig. 10